Electronic Version
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[MULTI-LEVEL MEMORY CELL]

Abstract

A multi-level memory cell including a substrate, a tunneling dielectric layer, a charge-trapping layer, a top dielectric layer, a gate and a pair of source/drain regions is provided. The tunneling dielectric layer, the charge-trapping layer and the top dielectric layer are sequentially formed between the substrate and the gate. The top dielectric layer has at least two portions, and the top dielectric layer in each portion has a different thickness. The source/drain regions are disposed in the substrate on each side of the gate. Since the thickness of the top dielectric layer in each portion is different, the electric field strength between the gate and the substrate when a voltage is applied to the memory cell are different in each portion. With the number of charges trapped within the charge-trapping layer different in each portion, a multiple of data bits can be stored within each memory cell.